Highly Elastic Gold Passivated Mechanically Flexible Interconnects

Chaoqi Zhang, *Student Member, IEEE*, Hyung Suk Yang, *Student Member, IEEE*,
and Muhannad S. Bakir, *Senior Member, IEEE*

Abstract—A wafer-level batch fabricated mechanically flexible interconnect (MFI) technology with 65-μm vertical elastic range of motion is experimentally demonstrated. A metal alloy (NiW) with ultrahigh yield strength and enhanced geometrical design is adopted to enable elastic deformation over the entire vertical range of motion. The enhanced geometrical design of the MFIs ensures that the stress is distributed uniformly during deformation, and simultaneously maintains an inner stress that is lower than the yield strength of NiW during vertical deformation. In addition, the MFIs are passivated with gold, which is experimentally verified to not only lower the electrical resistance, but also significantly extends the lifetime of the MFIs as it eliminates oxidation of NiW. For 10-μm-thick Au-NiW MFIs, the contact force is up to 10 mN at 50-μm elastic vertical deformation (i.e., compliance of 5 mm/N).

Index Terms—CMOS/MEMS integration, flexible interconnects, gold passivation layer, NiW, packaging.

I. INTRODUCTION

WITH the rapid growth of portable electronics as well as high-performance computing systems, combined with the ever growing set of challenges in sustaining performance gains from CMOS scaling, novel system interconnection, and integration platforms have emerged as a key enabler to the next era of electronics. This trend is well demonstrated in recent published advances. For example, a novel integrated microsystem platform was recently developed by Xilinx in which silicon interposers are used to enable high-density wiring between dice to circumvent the challenges in manufacturing large capacity field-programmable gate arrays and low-density wiring on conventional organic packages [1], [2]. A second example is the ever growing interest in 3-D IC integration (see [3]), which provides heterogeneous integration, improved performance, and reduced power. Yet a third example is the novel use of silicon nanophotonics to interconnect chips in a system to provide seamless interconnection through the use of low-energy massive off-chip bandwidth [4], [5]. The opportunities for disruptive electronic systems become even
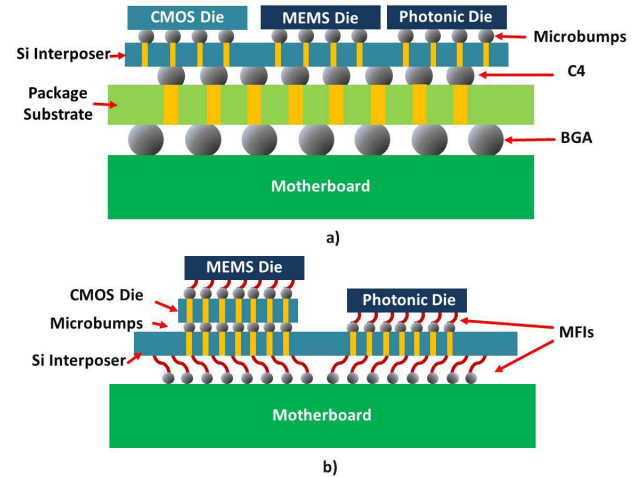

Fig. 1. Assembly of a Si interposer on the motherboard realized by (a) inserting an organic package substrate and (b) MFIs assisted direct mounting.

more exciting when one begins to combine all these advances together.

As shown in Fig. 1(a), when silicon interposers are used, a secondary package substrate is typically inserted to fan out the high density I/Os (C4 bumps) on the interposer to the low-density ball grid array I/Os on the motherboard. A second reason for the need of the secondary package substrate is due to the challenges associated with the coefficient of thermal expansion mismatch between a large silicon interposer and an organic motherboard. In addition, surface nonuniformity and the limited minimum feature size of organic motherboard technology are additional examples of major challenges associated with direct silicon interposer bonding to the motherboard.

The insertion of the package substrate, however, increases the system form factor and also degrades electrical performance. Therefore, there is a need in some applications to directly mount the silicon interposer to the motherboard, as shown in Fig. 1(b). The vision is to have the silicon die be bonded on the interposer. Next, redistribution layer on the interposer would connect to through silicon vias (TSVs). The TSVs would then make electrical interconnection to the motherboard using mechanically flexible interconnects (MFIs). This is especially important for thin mobile device applications where low profile of the electronic components is paramount. In addition, this can potentially enable the elimination of the package-level interconnects, thereby improving signaling performance and lowering energy dissipation of the overall system (Fig. 1). In this paper, we explore the design and

fabrication of high vertical range of motion MFIs to enable direct mounting of a silicon interposer to the motherboard.

II. REQUIREMENTS FOR MFIs

To address the challenges in assembling a Si chip to an organic substrate, various forms of MFIs have already been proposed and demonstrated. These includes: 1) flexible interconnects formed on or within a low-modulus polymer substrate, such as the wide area vertical expansion package [6], Floating Pads Technology [7], and sea of leads [8]; 2) modified wire-bond based technology, such as MicroSpring technology [9]; 3) stress engineered metal interconnects, such as rematable spring interconnect [10], J-spring [11], and coiled microspring [12]; and 4) 3-D free standing microspring technology, such as β-helix [13], G-helix [14], flex-connects [15], nickel tungsten (NiW) microsprings [16], and curved copper compliant die-package interconnects [17]. A novel copper-based 3-D curved MFI technology was previously reported by Yang *et al.* [18], [19]. Despite using a tapered and curved geometrical profile to uniformly distribute and reduce the maximum stress during deformation, the low-yield strength of the material used, Cu (yield strength of 200 MPa [20]), makes it difficult to extend the vertical elastic range of deformation beyond 20 μm. This material limitation was overcome recently by the use of NiW, which has a significantly higher yield strength (as high as 1.9 GPa [21]). The usefulness of the material was demonstrated in [16], [21], where flexible interconnects with a larger vertical elastic range of deformation (up to 40 μm) were developed and demonstrated. However, due to the readily oxidizing nature of Cu as well as NiW, it has not yet been shown that it can be used in real applications with a reasonable reliability, especially in applications where the interconnect structures are not encapsulated in an inert environment.

Other than using MFIs to interconnect an interposer to a motherboard directly, a wide range of applications exist for MFIs. For example, MFI technology is promising in probe cards for wafer-level testing as well as in rematable electronic applications [22]. Therefore, to develop MFIs that can be effective in the various applications listed above, four key requirements must be fulfilled: 1) fine pitch high density interconnects; 2) large elastic vertical deformation for sufficient flexibility and reusability; 3) high contact force for low-contact resistance temporary interconnection; and 4) long lifetime (for usefulness and reliability). These four listed requirements are adopted for the design of the MFIs in this paper. Specifically, we extend the work of Yang *et al.* using NiW to attain up to 65 μm of elastic vertical deformation. In addition, the MFIs are coated using an electroless gold plating process, which preserves the mechanical and electrical characteristics of the MFI during their field use (i.e., addresses the NiW oxidation challenge).

III. DESIGN OF MFIs

To maintain the MFIs within the elastic deformation regime, the maximum internal stress of the freestanding interconnect during deformation should not exceed the yield strength of the material. Therefore, fabricating MFIs using a material with high yield strength is a cornerstone to the design of MFIs.

An optimized geometry should also be considered to maximize the range of elastic deformation. As discussed in the previous research of Yang *et al.* [18], [19], thinner and longer MFIs help in decreasing the internal stress and maintaining a maximum stress value that is below the yield strength of the MFIs material for a given deformation range. Both the thickness and length of the MFIs, however, cannot be manipulated easily as they will be constrained by practical, electrical, and mechanical performance requirements. Thinner MFIs lead to lower contact force, and given that a relatively large contact force is necessary for applications that require temporary interconnection, thicker MFIs are required to ensure reliable electrical interconnection (i.e., low contact resistance). In addition, to achieve high-bandwidth interconnections, a high I/O density is desirable in many applications, which implies that shorter MFIs are needed. Therefore, instead of thinning and elongating the MFIs, an optimized width profile is adopted to lower the maximum internal stress while maintaining a large contact force. Below, we elaborate on the key points above.

A. High Yield Strength Metal Alloy-NiW

Cu has been used extensively for various flexible interconnect technologies [6]–[9], [11]–[15], [17]–[19] because of the high conductivity, high electromigration resistance, and established low-cost electroplating techniques. The yield strength of Cu is, however, relatively low (<200 MPa [21]). Thus, it limits the range of elastic deformation. Tungsten, on the other hand, has a yield strength of up to $\sim$1.37 GPa [23]. It, however, cannot be efficiently deposited using electroplating, which is the most convenient low-cost method to deposit thick metal film (few micrometer and above) at room temperature.

NiW, a Ni alloy with nanocrystal structure developed in [16], [20], is an ideal material for MFIs due to its high yield strength of up to $\sim$1.9 GPa and its ability to be deposited using electroplating. Besides the high yield strength, which is critical for large elastic deformation, the latter is also particularly important for low-cost manufacturing since a thick metal layer is typically needed.

B. Tapered MFI Design

A tapered MFI width design based on the principles developed by Yang *et al.* [18], [19] is used here to distribute the stress uniformly and provide larger vertical range of motion. Finite element method (FEM) simulations of the stress distribution within a tapered NiW MFI with 50-μm vertical deformation are shown in Fig. 2. The simulated MFI is 9-μm thick and occupies a footprint of 120-μm by 200 μm. The FEM simulations performed by ANSYS Workbench software package show that at 50-μm vertical deformation, the maximum local von Mises stress is 2.06 GPa, which is close to the yield strength of NiW. The simulated reaction force at this value of deformation is 6.0 mN.

Since the gold passivation layer is very thin (≤ 0.5 μm) and soft compared with NiW, the impact of the gold passivation
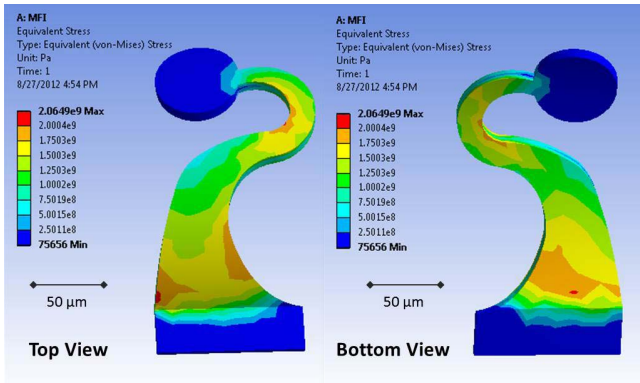
Fig. 2. Von Mises stress FEM simulation of 50-μm vertically deformed NiW MFI. Inner stress is uniformly distributed.
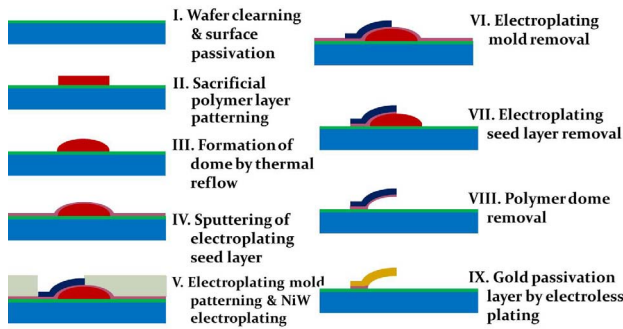

Fig. 3. Process flow for Au-NiW MFIs.

layer on the mechanical deformation of the MFI is neglected in the simulations, which is verified experimentally in Section V.

IV. FABRICATION PROCESS

The fabrication of the flexible interconnects, as shown in Fig. 3, is similar to the Cu-based MFI process described in [19] and [20], and similarly, this process requires only two photolithography steps. The first photolithography step is used to pattern a sacrificial polymer layer on the substrate, which transforms into a dome following a thermal reflow process. The second photolithography step is used to pattern a photoresist electroplating mold on the surface of a Ti/Cu/Ti seed layer, which covers the sacrificial polymer. After the electroplating of the NiW MFIs, the electroplating mold, the seed layer, and sacrificial polymer dome are removed subsequently leaving behind free-standing MFIs with a 120 μm by 200-μm footprint and 65-μm z-axis gap, as shown in Figs. 4 and 5. Finally, a gold passivation layer is deposited on the free-standing MFIs using electroless plating. Below, we elaborate on the key process steps.

A. Sacrificial Polymer Dome

The height of the polymer dome determines the maximum vertical deformation range. Depending on the polymer dome thickness, single or multiple polymer spin coating steps may be needed. A single spin coat of the polymer layer was sufficient to attain the 20-μm vertical gap for the Cu MFIs in previous research [19]. To reach higher vertical gap, multiple coatings were used to obtain a 45-μm-thick polymer layer,
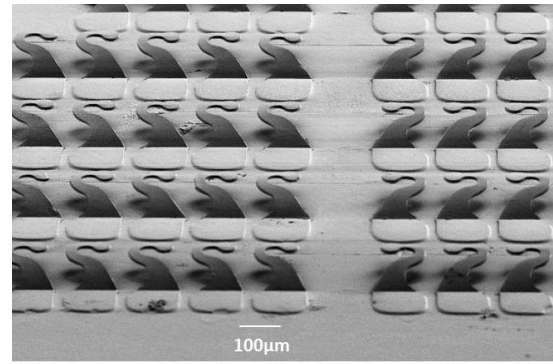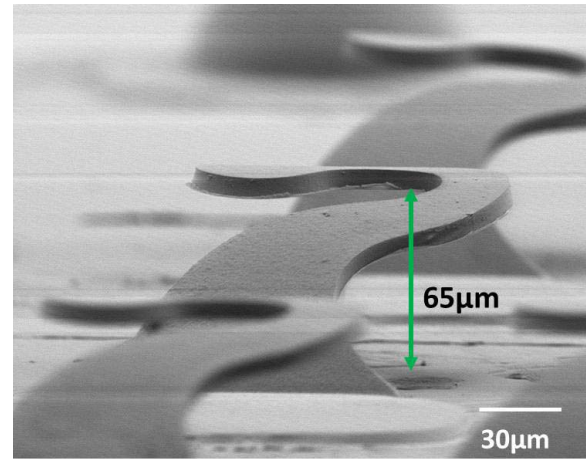

Fig. 4. Free standing Au-NiW MFIs.

Fig. 5. Gold passivated NiW MFIs with 65-μm vertical gap.

which after reflow, transforms into a polymer dome with a height of 65 μm. Since the sacrificial polymer dome is very thick, gradual post bake followed by natural cool down must be used to avoid solvent outgassing and polymer dome cracking.

B. Electroplating Mold

To form MFIs by electroplating, > 50-μm-thick conformal photoresist film needs to be coated and patterned on the Ti/Cu/Ti seed layer covering the substrate with polymer domes. Note that the polymer domes result in 65-μm surface variation. The main challenge in the formation of the electroplating mold is dose control. This is true because after spin coating, the thickness of the photoresist layer on the peak of the domes is thinner than the photoresist thickness in the valley between the domes. Thus, the variation of photoresist thickness leads to different dose requirements for exposure across the wafer. Since the photoresist is very sensitive to under exposure, which typically occurs in the valley, and since it is the thickest photoresist region, the exposure dose for the whole wafer is tuned based on the requirement of the valley.

C. Electroplating and Release

Since the yield strength of Cu is too low to afford the large vertical range of motion, NiW is used to form the MFIs using electroplating, which is a fast, low cost, and CMOS compatible
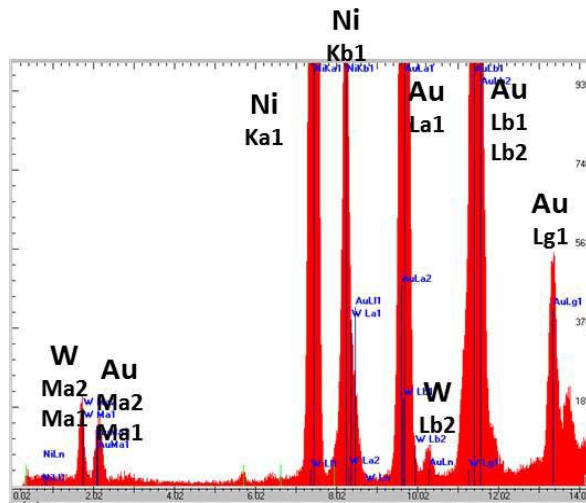
Fig. 6.   Au-NiW MFIs components verification by XRF.

approach. Traditional Ni sulphate-based NiW electroplating electrolytes require high electroplating temperature (~ 90 °C) and harsh alkaline solution (pH $\geq$ 8), which may not be compatible with some Si processing. In addition, the internal stress of NiW electrodeposited by a Ni sulphate-based bath is high and can easily lead to cracks. Therefore, Ni sulfamate-based electrolytes are used in this paper. The components of NiW MFIs with gold passivation layer are verified by X-ray fluorescence (XRF), as shown in Fig. 6.

For a given bath temperature and pH value, the thickness of MFIs is mainly controlled by the electroplating time. Since MFIs with various thickness values were formed in different batches for testing, the MFIs thickness will be clearly noted along all data reported in the following sections.

After electroplating, the polymer dome and seed layer are removed to yield 3-D free standing NiW MFI with a footprint of 200 μm by 120 μm (Fig. 4) and vertical gap of 65 μm (Fig. 5).

D. Electroless Gold Passivation Layer

The passivation layer, which determines the durability of the lead, is critical for flexible interconnects. For both Cu and NiW MFIs, oxidation and corrosion of the exposed metal to the ambient will significantly shorten the MFIs lifetime. Therefore, a passivation layer is mandatory for MFIs exposed to the ambient to preserve the mechanical and electrical properties during their lifetime.

As shown in Fig. 7, a gold passivation layer is deposited on the surface of the NiW MFIs by electroless plating. Since the deposited gold results from a chemical reaction on all conductive surfaces, as shown in Fig. 7, all exposed MFI surfaces are passivated as required in this application. One of the gold passivated NiW MFIs was flipped using tweezers (large force was applied to detach the MFI) to illustrate the passivation layer uniformity (Fig. 7). The only uncoated part of the MFI, as expected, is the unexposed interface between the anchor of the MFI and the substrate. Compared with other methods for passivation (e.g., polymer coating) there are significant benefits: 1) simple and low-cost processing since
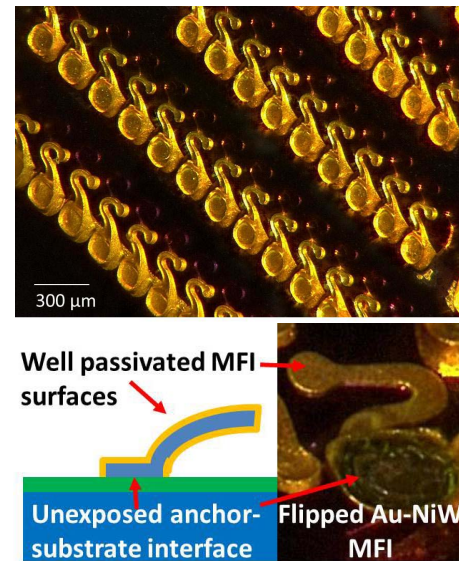

Fig. 7.   Optical micrograph images of MFIs with 65-μm vertical gap after electroless gold passivation.
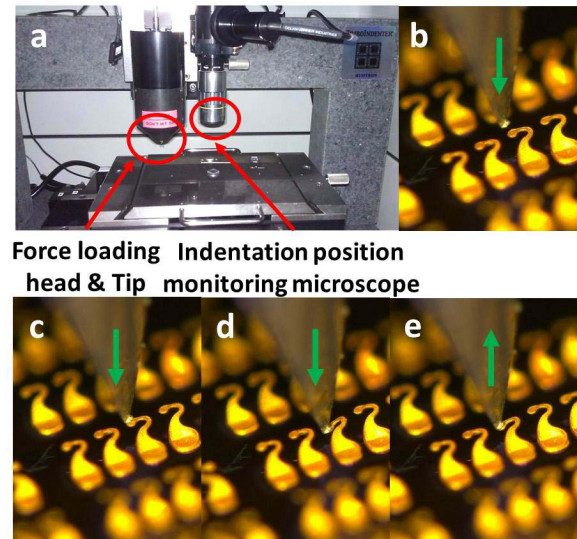

Fig. 8.   Indentation tests of MFIs are carried out by Hysitron Triboindenter. Each indentation cycle includes tip contact to MFI, MFI deformation, and tip release from MFI (b-e). The free standing MFI is deformed downward (c) to a preset depth (d) under a prede.ned force pro.le applied by a piezo-driven tip followed by a force release (e).

photolithography is not needed; 2) high conductance, which is important in lowering the MFI resistance, especially for NiW MFI; and 3) longer lifetime.

V. RESULTS AND DISCUSSION

A. Mechanical Characterization

Multiple indentations were employed to determine the mechanical properties of Au-NiW MFIs, including the maximum elastic deformation range and the corresponding contact force and compliance. The results of the mechanical characterization of the MFIs are reported in this section.

1) Indentation Test of NiW MFIs With Gold Passivation Layer: Indentation testing of the MFIs was carried out using
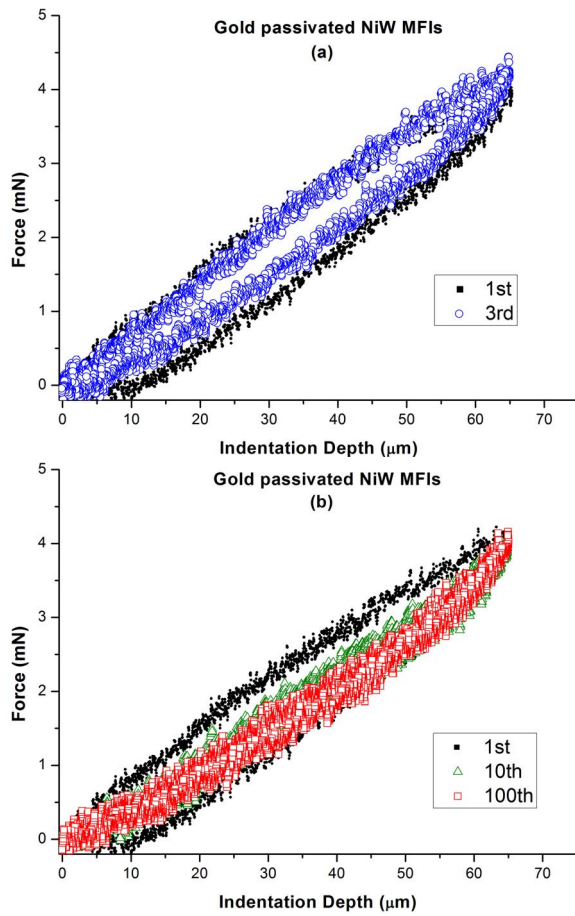
Fig. 9. Results from 100 indentations of a single gold passivated NiW MFI. Plots illustrate elastic deformation up to 65 μm. (a) shows that the first few indentation cycles do not overlap with each other which is believed caused by minor defects generated during the fabrication process, such as NiW electroplatin. Once these defects are recovered after the first several indentations, subsequent indentation profiles shown in (b) are almost identical.
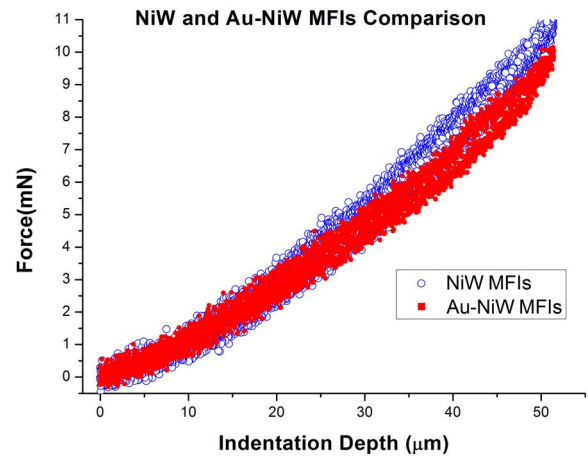

Fig. 10. Comparison between (top) NiW MFI and (bottom) Au-NiW MFI shows that the gold electroless passivation layer does not degrade the elastic deformation of the NiW MFIs.
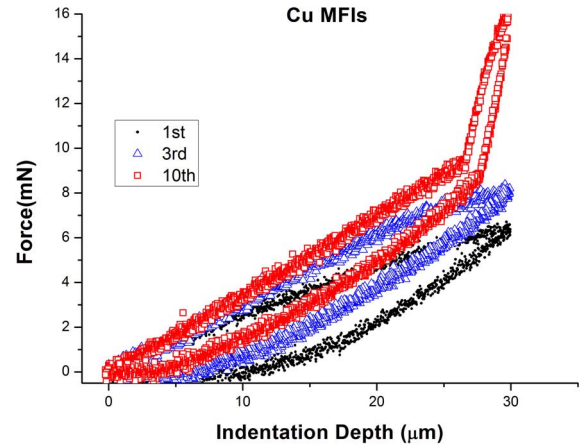

Fig. 11. Cu MFI with similar thickness (11 μm) cannot provide 30-μm elastic deformation.

a Hysitron TriboIndenter, as shown in Fig. 8(a). For each indentation cycle, the free standing MFI is deformed downward to a preset depth [Fig. 8(b)–(d)] under a predefined force profile applied by a piezo-driven tip followed by a force release [Fig. 8(e)]. The real-time position and the corresponding reaction force of the piezo-driven tip, which has the same value as that of the MFI, are recorded.

The results recorded in Fig. 9 verify that the 65-μm vertical deformation is elastic (the MFI thickness is 6.85 μm). Fig. 9(a) shows that the first few indentation cycles do not overlap with each other. This is believed to be caused by some plastic deformation that occurs in the first several indentation cycles. These might be caused by minor defects generated during the fabrication process, especially during NiW electroplating. Once these defects are recovered after the first several indentations, subsequent indentation profiles shown in Fig. 9(b) are almost identical (roughly, from the tenth cycle to the hundredth). As discussed in the previous section, to increase the contact force thicker NiW MFIs should be used, which can be easily accomplished by increasing the electroplating time of NiW film.

As discussed in the previous section, since the MFI design was optimized without the gold layer, MFIs before and after gold passivation were indented to verify that the electroless gold film does not degrade the elastic deformation of the NiW MFIs.

The results of 100 indentation test cycles on NiW MFIs before and after gold passivation are compared in Fig. 10. The anchor thickness of the indented NiW MFI in this experiment is 10.12 μm, and the corresponding contact force for 50-μm deformation is 10.8 mN (i.e., compliance of 4.63 mm/N). Before deposition of the gold passivation layer, the NiW MFIs were first cleaned with diluted HCl to remove the native oxide from the NiW layer. The anchor thickness of the HCl cleaned MFI is 9.43 and 9.73 μm before and after electroless gold plating, respectively. This indicates that 0.3 μm of electroless gold was deposited. Since both sides of the free-standing MFI are coated with gold, the total thickness of MFI is ~10.03 μm (i.e., 0.3 μm of gold on both the top and bottom sides of the MFI). With the measured indentation results in Fig. 10, the corresponding contact force for 50-μm deformation is 10 mN (i.e., compliance of 5 mm/N). Comparison of the two indentation results shown in Fig. 10 confirms the assumption that the impact of the electroless gold passivation layer/process appears to be negligible.
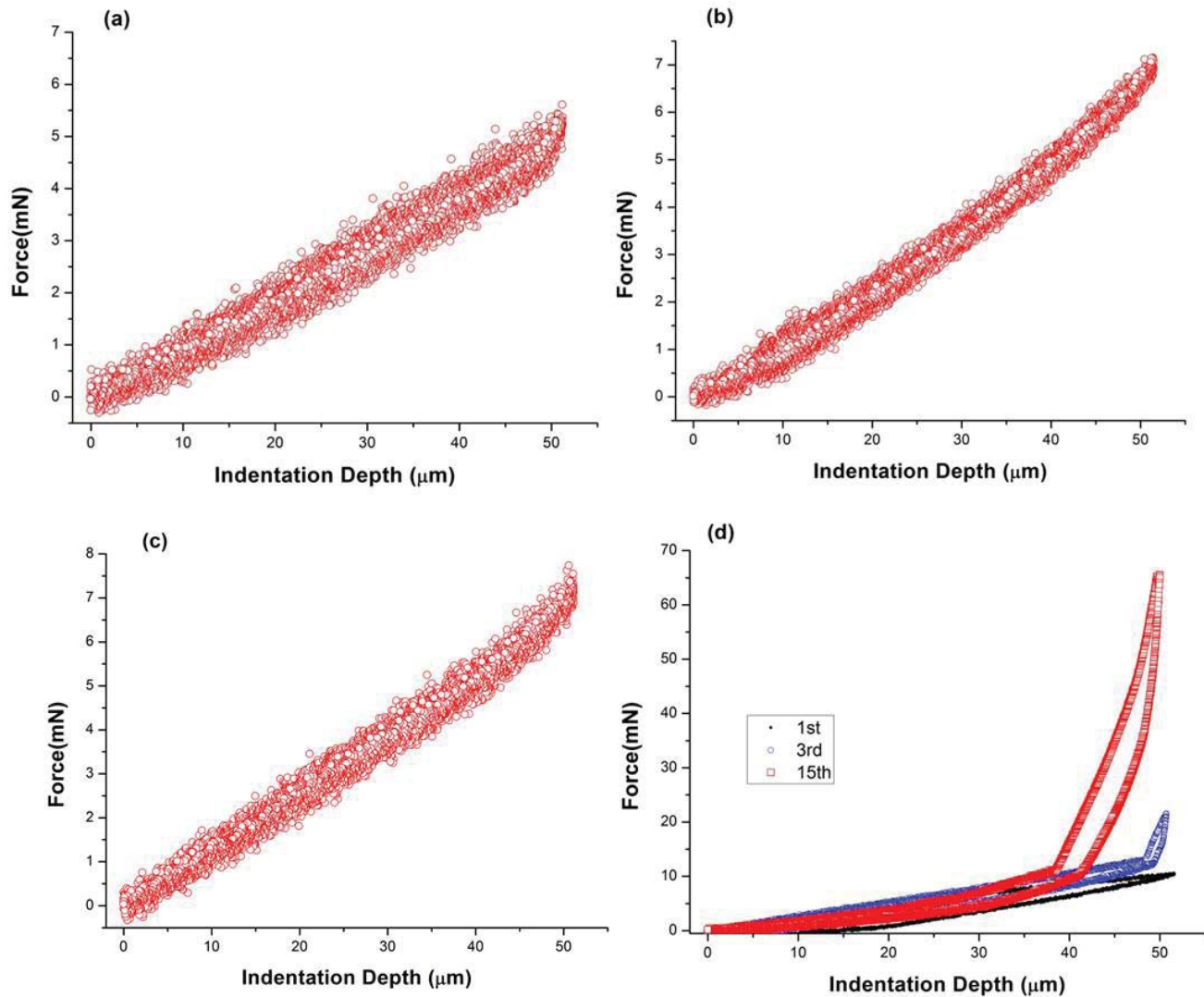
Fig. 12. Life-time verification of NiW MFIs with gold passivation layer. NiW MFIs with gold passivation layer maintain the 50-μm elastic deformation capability after two months, unlike the nonpassivated NiW MFIs. (a) Gold passivated NiW MFIs. (b) Gold passivated NiW MFIs (after two months). (c) NiW MFIs without gold passivation layer. (d) NiW MFIs without gold passivation layer (after two months).

2) Cu MFIs: To compare the Au-NiW MFIs with Cu-based MFIs, 100 indentation test cycles were also performed on Cu MFIs of the same design. In this case, the copper MFI was 11-μm thick.

The Cu MFIs were, however, plastically deformed within 30-μm deformation. As shown in Fig. 11, the forward and backward plots are not overlapping, and the contact force is not linear with indentation depth. In addition, there are clear indentation depth intercepts shown in the first and third indentation plots in Fig. 11, which show that the MFI end position is lower than the starting position of each indentation cycle. For example, in the first indentation cycle, the contact force becomes zero when the indentation depth is 10 μm, which means that when the piezo-driven tip does not contact the MFI any more, the MFI is ~10-μm lower than the starting position. Therefore, the vertical gap of the MFI continues to shrink due to plastic deformation. At the end of the tenth indentation cycle, the tip of the MFI touches the substrate surface resulting in the contact force increasing at a much larger slope than before experiments.

3) Improved Life Time: As mentioned earlier, without the passivation layer protecting NiW from oxidation, the performance of flexible interconnects degrades significantly with time. To verify the lifetime improvement due to the electroless gold passivation layer, 100 indentation test cycles were carried out on NiW MFIs with and without gold passivation. The indentations were performed on the same samples after two months of storage in room temperature with relative humidity of 42%. Fig. 12(a) and (b) shows that after two months, the Au-NiW MFIs maintain elastic deformation. The original 50-μm elastic deformation capability of NiW MFIs without a gold passivation layer, however, cannot be maintained, as shown in Fig. 11(c) and (d). Obvious plastic deformation is observed from the indentation results of the NiW MFIs shown in Fig. 11(d). In addition, the intercept on the indentation depth axis of the backward plot shows that the tip of the deformed MFI does not return to the starting position of each cycle. The vertical gap was shrunk to < 50 μm (from 65-μm initial gap) after the first two cycles and the tip began to touch the substrate at the end of third cycle.
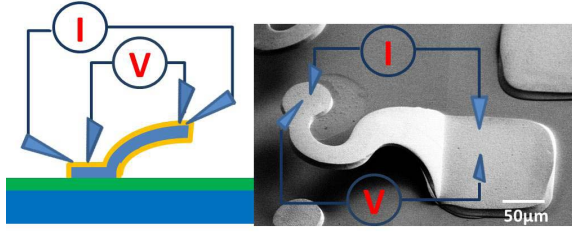
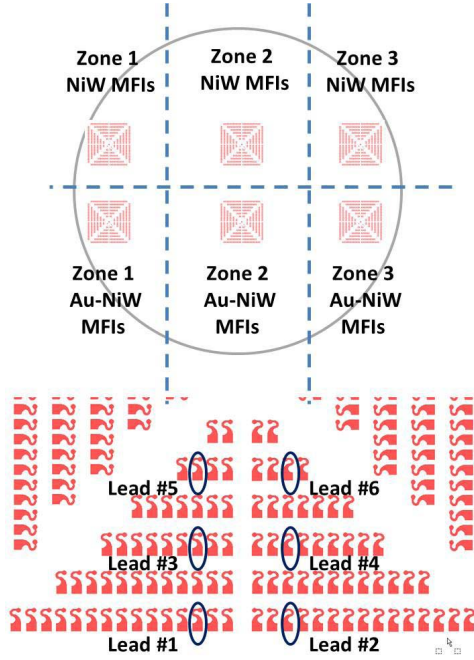Fig. 13.   Four-point resistance measurement of MFIs.

Fig. 14.   Electrical resistance measurement test.

B. Electrical Characterization

Four point probing was used to perform MFI electrical resistance measurements, as shown in Fig. 13. During the measurements, the tested MFIs are partially bent to attain a stable resistance reading. The average resistance of 10.25-μm-thick NiW MFI is 101.62 mΩ. This value is higher than the FEM simulated electrical resistance in ANSYS, which was 78.1 mΩ. This difference is believed to be caused by the contact resistance since the partially deformed MFI cannot provide large enough contact force to sufficiently break the thin native oxidation layer on the MFI surface.

The measured resistance of the gold passivated MFIs (0.3-μm gold layer thickness on each side of the MFI) is 67.8 mΩ. The gold passivation layer reduces the resistance due to: 1) the high conductivity gold layer is in parallel to the NiW film and 2) provides a nonoxidized contact surface between the probe tip and the MFI. Of course, forming a thicker MFI is another approach to lowering the electrical resistance of the MFI. Given a target deformation depth, the larger contact force provided by thicker MFI is also desirable. However, as discussed in Section III, additional design effort is needed to ensure that the maximum internal stress is lower than the yield strength of the material.

TABLE I
ELECTRICAL RESISTANCE MEASUREMENT FOR NiW MFIS

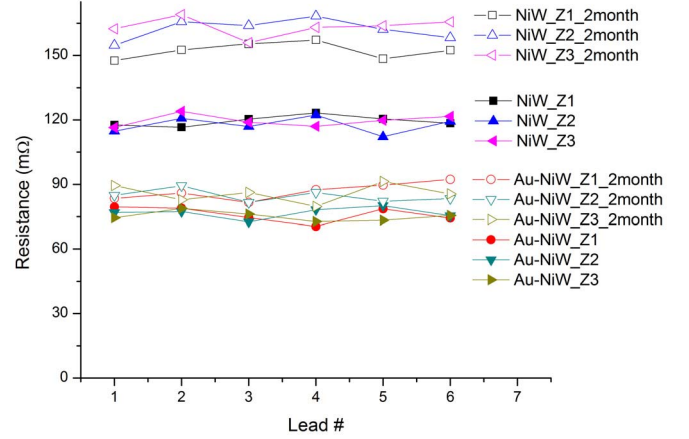|	Zone_1(mΩ)		Zone 2(mΩ)		Zone 3(mΩ)	
	No Au	Au	No Au	Au	No Au	Au
t=0	119.5	76.1	117.7	76.7	119.6	75.2
t=2 months	152.3	86.7	162.2	84.6	163.3	85.8

Fig. 15.   Electrical resistance measurements of NiW and Au-NiW MFIs. As can be seen, the gold passivated MFIs preserved their electrical resistance over a two-month period.

Similar to the lifetime testing reported in the last section, four point probing was carried out over a two-month period to compare the electrical resistance of the MFIs. As shown in Fig. 14, the whole wafer was separated into three zones, and each zone was divided into two subzones (one with and one without gold passivation). Six MFIs, numbered 1–6 in Fig. 14, were measured by four-point probing method and then stored in room temperature with relative humidity of 42%. After two months, another set of measurements was performed for comparison. All the electrical resistance measurements of the NiW and Au-NiW MFIs are summarized in Table I and Fig. 15. The average resistance of 9.12-μm-thick NiW MFIs increased from a range of {117.7–119.6} mΩ to a range of {152.3–163.3} mΩ. Thus, there is on average a 39.15 mΩ change in resistance. For the gold passivated MFI, the change of average resistance is < 10 mΩ.

VI. CONCLUSION

Wafer-level batch fabricated gold passivated NiW MFIs are experimentally demonstrated with 65-μm vertical elastic range of motion. The adoption of electroplated high yield strength NiW and the curved and tapered MFI design profile ensures that the 65-μm deformation is elastic. In addition, the electroless gold passivation layer not only lowers the resistance, but was also critical to protecting the MFIs from oxidation to preserve their mechanical and electrical characteristics, which was experimentally verified by the results of 100 indentations and four-point electrical resistance measurements, respectively, performed over a period of two months.

REFERENCES

[1] B. Banijamali, K. Nagarajan, and S. Ramalingam, "Assembly and reliability challenges in 3D integration of 28 nm FPGA die on a large high density 65 nm passive interposer," in *Proc. IEEE 62nd ECTC*, Jun. 2012, pp. 279–283.

[2] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28 nm technology FPGA," in *Proc. IEEE 61st ECTC*, Jun. 2011, pp. 285–290.

[3] R. Yarema, R. Yarema, G. Deptuch, J. Hoff, A. Shenai, M. Trimpl, T. Zimmerman, M. Demarteau, R. Liptona, and D. Christian, "3D design activities at Fermilab—Opportunities for physics," *Nuclear Instrum. Methods Phys. Res. Section A, Accel., Spectrometers, Detectors Assoc. Equip.*, vol. 617, nos. 1–3, pp. 375–377, May 2010.

[4] H. D. Thacker, Y. Luo, J. Shi, I. Shubin, J. Lexau, X. Zheng, G. Li, J. Yao, J. Costa, T. Pinguet, A. Mekis, P. Dong, S. Liao, D. Feng, M. Asghari, R. Ho, K. Raj, J. G. Mitchell, A. V. Krishnamoorthy, and J. E. Cunningham, "Flip-chip integrated silicon photonic bridge chips for sub-picojoule per bit optical links," in *Proc. 60th ECTC*, Jun. 2010, pp. 240–246.

[5] I. Shubin, I. Shubin, H. D. Thacker, J.-H. Lee, G. Li, X. Zheng, J. Lexau, R. Ho, J. G. Mitchell, Y. Luo, J. Yao, K. Raj, and A. V. Krishnamoorthy, "Scaling hybrid-integration of silicon photonics in freescale 130 nm to TSMC 40 nm-CMOS VLSI drivers for low power communications," in *Proc. IEEE 62nd ECTC*, Jun. 2012, pp. 1518–1525.

[6] Y.-G. Kim, I. Mohammed, B.-S. Seol, and T.-G. Kang, "Wide area vertical expansion (WAVE) package design for high speed application: Reliability and performance," in *Proc. 51st ECTC*, Jun. 2001, pp. 54–62.

[7] R. Fillion, R. Wojnarowski, H. Colc, and G. Claydon, "On-wafer process for stress-free area array floating pads," in *Proc. Int. Symp. Microelectron.*, 2001, pp. 100–105.

[8] M. S. Bakir, H. A. Reed, H. D. Thacker, G. S. Patel, P. A. Kohl, K. P. Martin, and J. D. Meindl, "Sea of leads (SoL) ultra high density wafer level chip input/output interconnections for gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2039–2048, Oct. 2003.

[9] N. L. Tracy, R. Rothenberger, C. Copper, N. Corman, G. Biddle, A. Matthews, and S. McCarthy, "Array sockets and connectors using microspring technology," in *Proc. 26th IEEE/CPMT Int. Electron. Manuf. Symp.*, Oct. 2000, pp. 129–140.

[10] I. Shubin, E. M. Chow, J. Cunningham, D. De Bruyker, C. Chua, B. Cheng, J. C. Knights, K. Sahasrabuddhe, Y. Luo, A. Chow, J. Simons, A. V. Krishnamoorthy, R. Hopkins, R. Drost, R. Ho, D. Douglas, and J. Mitchell, "Novel packaging with rematable spring interconnect chips for MCM," in *Proc. 59th ECTC*, May 2009, pp. 1053–1058.

[11] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-Springs - innovative compliant interconnects for next-generation packaging," in *Proc. 52nd ECTC*, 2002, pp. 1359–1365.

[12] R. B. Marcus, "A new coiled microspring contact technology," in *Proc. 51st ECTC*, Jun. 2001, pp. 1227–1232.

[13] Q. Zhu, M. Lunyu, and S. K. Sitaraman, "β-Helix: A lithography-based compliant off-chip interconnect," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 3, pp. 582–590, Sep. 2003.

[14] Q. Zhu, M. Lunyu, and S. K. Sitaraman, "Design and optimization of a novel compliant off-chip interconnect one-turn helix," in *Proc. 52nd ECTC*, 2002, pp. 910–914.

[15] K. Kacker, T. Sokol, and S. K. Sitaraman, "FlexConnects: A cost-effective implementation of compliant chip-to-substrate interconnects," in *Proc. 57th ECTC*, Jun. 2007, pp. 1678–1684.

[16] G. Spanier, C. Kruger, U. Schnakenberg, and W. Mokwa, "Platform for temporary testing of hybrid microsystems at high frequencies," *J. Microelectromech. Syst.*, vol. 16, no. 6, pp. 1367–1377, Dec. 2007.

[17] S. Muthukumar, C. D. Hill, S. Ford, W. Worwag, T. Dambrauskas, P. C. Challela, T. S. Dory, N. M. Patel, E. L. Ramsay, and D. S. Chau, "High-density compliant die-package interconnects," in *Proc. 56th ECTC*, 2006, pp. 1233–1238.

[18] H. S. Yang and M. S. Bakir, "3D integration of CMOS and MEMS using mechanically flexible interconnects (MFI) and through silicon vias (TSV)," in *Proc. 60th ECTC*, Jun. 2010, pp. 822–828.

[19] H. S. Yang and M. S. Bakir, "Design, fabrication, and characterization of freestanding mechanically flexible interconnects using curved sacrificial layer," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 2, no. 4, pp. 561–568, Apr. 2012.

[20] M. B. Renee and C. W. Robert, "Fiber pullout behavior and impact toughness of short shaped copper fibers in thermoset matrices," *Composites A, Appl. Sci. Manuf.*, vol. 36, no. 5, pp. 683–690, May 2005.

[21] E. Slavcheva, W. Mokwa, and U. Schnakenberg, "Electrodeposition and properties of NiW films for MEMS application," *Electrochim. Acta*, vol. 50, no. 28, pp. 5573–5580, Sep. 2005.

[22] H. Yang, R. Ravindran, M. S. Bakir, and J. D. Meindl, "A 3D interconnect system for large biosensor array and CMOS signal-processing IC integration," in *Proc. IITC*, Jun. 2010, pp. 1–3.

[23] P. L. Raffo, "Yield and fracture in tungsten and tungsten-rhenium alloys," in *Technical Note*, Washington, DC, USA: NASA, May 1968.

Chaoqi Zhang (S'12) received the B.S. degree in physics from Shandong University, Shandong, China, in 2005, and the M.S. degree in microelectronics from Tsinghua University, Beijing, China, in 2008. He is currently pursuing the Ph.D. degree in electrical engineering with the Georgia Institute of Technology, Atlanta, GA, USA. His current research interests include flexible interconnect technologies for 2.5-D/3-D heterogeneous integration.

Hyung Suk Yang (S'07) received the B.S. (High Honor) degree in computer engineering and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2007 and 2008, respectively.

His current research interests include 3-D heterogeneous integration using novel microfabricated interconnect technologies. He is the author or co-author of 15 journal publications and conference proceedings.

Mr. Yang is co-recipient of the 2009 and 2010 SRC TECHCON Best in Session Paper Award, the 2009 IMAPS Best Student Paper Award, and the 2009 IMAPS Best in Session Paper Award. He is a recipient of the Intel Corporation Ph.D. Fellowship for 2011 to 2012, and is a reviewer for the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY and the IEEE TRANSACTIONS ON ELECTRONICS PACKAGING TECHNOLOGY.

Muhannad S. Bakir (SM'12) received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2003.

He is currently an Associate Professor and the ON Semiconductor Junior Professor with the School of Electrical and Computer Engineering, Georgia Tech. He is an Editor of *Integrated Interconnect Technologies for 3-D Nanoelectronic Systems* (Artech House, 2009).

Dr. Bakir was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium and has been awarded the 2013 Intel Early Career Faculty Honor Award and the 2012 DARPA Young Faculty Award. He is a recipient of the 2011 IEEE Components, Packaging and Manufacturing Technology Society Outstanding Young Engineer Award. He is a member of the International Technology Roadmap for Semiconductors Technical Working Group for Assembly and Packaging.